

TRANSFORMERLESS DC-TO-DC CONVERTERS WITH LARGE CONVERSION RATIOS

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ABSTRACT

A new switching dc-to-dc converter is introduced in which large voltage step-down ratios can be achieved without a very small duty ratio and without a transformer. The circuit is an extension of the Cuk converter to incorporate a multistage capacitor divider. A particularly suitable application would be a 50V to 5V converter in which dc isolation is not required. The absence of a transformer and a larger duty ratio permits operation at very high switching frequency, and makes the circuit amenable to partial integration and hybrid construction techniques.

An experimental three-stage voltage divider Cuk converter converts 50V to 5V at 50W with an efficiency of 77% at 500 kHz and 71% at 1 MHz, higher than for a basic Cuk converter operated at the same conditions.

1. INTRODUCTION

There is a growing need for a converter/regulator to provide +5V output from a nominal -48V input, and with low profile capable of assembly on a plug-in card. There is an obvious motivation to use a switching frequency at least in the hundreds of kHz, in order to reduce magnetics sizes and to take advantage of hybrid construction techniques. With the advent of power MOSFETs, the switching frequency is limited by the magnetics rather than by the switch.

More specifically, it is a transformer that limits the frequency, rather than an inductor, because the ratio of leakage to magnetizing

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A patent application has been filed on the voltage-divider Cuk converter circuit.

inductance increases as the physical size decreases. A transformer commonly provides two functions in a dc-to-dc switching converter: it provides dc isolation, and it provides an additional voltage conversion ratio over and above that available from the switch duty ratio.

In applications where dc isolation is not needed, a transformer (or an autotransformer) would normally still be required if the necessary voltage conversion ratio is large. For example, in a 50V-to-5V converter, the switch duty ratio would have to be about 0.1 if a transformer were not used, which severely limits the switching frequency and the dynamic range, and also has undesirable implications with respect to peak currents, loss of efficiency, and noise. On the other hand, if a transformer were used, the switching frequency would also be severely limited by the transformer itself.

This paper suggests a way to avoid both these undesirable solutions, by introduction of a voltage divider property that does not require a transformer.

2. THE VOLTAGE-DIVIDER CUK CONVERTER

The new circuit is another extension of the basic Cuk converter [1], introduced in 1976 as a solution to the problem of achieving nonpulsating current at both input and output with a minimum number of components. In the Cuk converter, shown in Fig. 1, the capacitor is charged by the input inductor current when the transistor is OFF and the diode is ON, and is discharged through the output inductor when the transistor is ON and the diode is OFF.

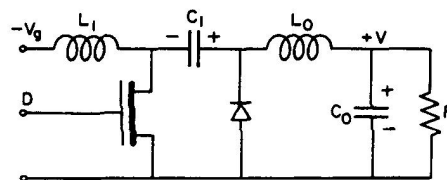


Fig. 1. The basic Cuk converter.

As far as the basic conversion property is concerned, the converter may be considered a coalesced boost followed by a buck converter, in which the capacitor average voltage V_C corresponds to the output of the boost stage, given by $V_g/(1-D)$, and also corresponds to the input of the buck stage whose output V is DV_C . Hence, the overall output-to-output conversion ratio is $M \equiv V/V_g = D/(1-D)$ where D is the fractional ON-time of the transistor and V_g is the input voltage. This is the same functional relationship as in the flyback converter, and permits either up or down conversion.

Polarity inversion between input and output occurs because during charge the positive capacitance terminal is grounded through the diode, and during discharge the negative end is grounded through the transistor. The circuit is normally designed to operate in the "continuous capacitance voltage mode" in which the polarity of the capacitance voltage does not reverse [2].

The Ćuk converter is unique compared with the conventional buck, flyback, and other converters in that it utilizes capacitive rather than magnetic energy transfer. It is this property that permits the capacitance voltage-divider feature to be incorporated. The new circuit, shown in its simplest form in Fig. 2, is a "voltage-divider Ćuk converter," in which two energy transfer capacitors

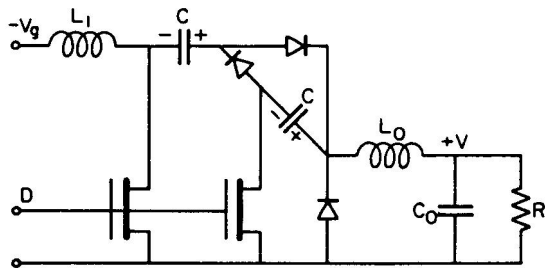


Fig. 2. The new voltage-divider Ćuk converter with two stages.

are charged in series when the transistors are OFF and discharged in parallel when the transistors are ON. Thus, effectively, a two-to-one voltage division is introduced, and the overall conversion ratio is $M = D/2(1-D)$ where D is the duty ratio of the two transistors driven ON and OFF simultaneously.

This concept can be generalized to where N capacitors are charged in series and discharged in parallel, as shown in Fig. 3, so that the overall conversion ratio is $D/N(1-D)$. The circuit configuration is shown in Fig. 4 for the two intervals that comprise the switching cycle. The transistors and diodes are assumed to be ideal switches. During the fractional OFF-time $(1-D)$ of the transistors, shown in Fig. 4(a), the N energy transfer capacitors are charged in series by the input current I_g . During the transistor fractional ON-time D , shown in Fig. 4(b), each capacitor

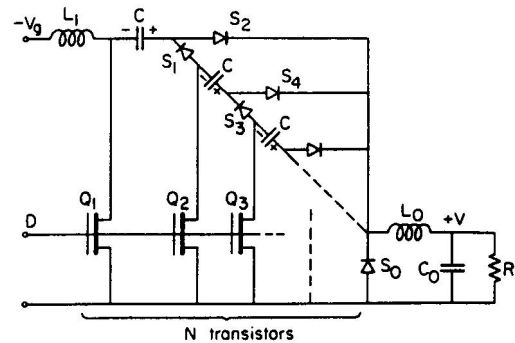


Fig. 3. Generalized N -stage voltage-divider Ćuk converter.

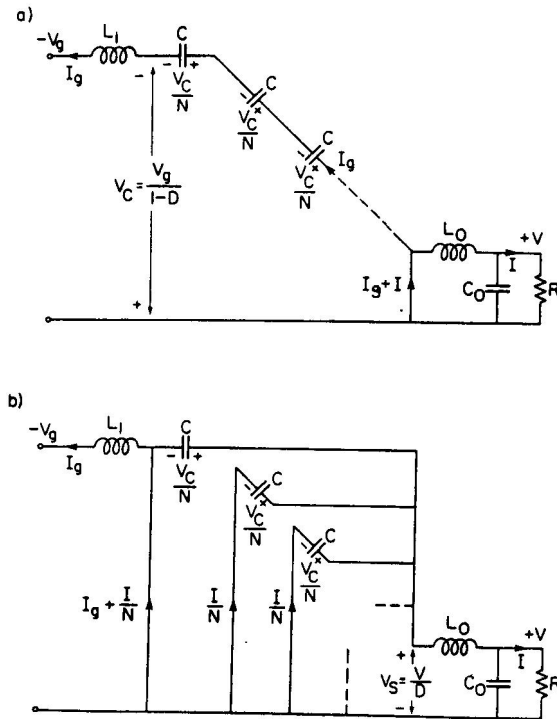


Fig. 4. N -stage converter: (a) during driving transistor OFF-time, N capacitors are charged in series; (b) during transistor ON-time, N capacitors are discharged in parallel.

supplies one N th of the output current I . By volt-second balance across the input inductor L_1 , the voltage across all N capacitors in series is $V_C = V_g/(1-D)$ (the same expression as for the basic Ćuk converter), and this voltage is shared equally by the N capacitors as a result of automatic self-adjustment when the capacitors are paralleled during the transistor fractional ON-time D .

In comparison with the basic Ćuk converter, the new converter operates at a higher duty ratio for the same overall conversion ratio $M = V/V_g$. The relation between the respective duty ratios D_N and D_1 is obtained from

$$\frac{D_N}{N(1-D_N)} = M = \frac{D_1}{1-D_1} \quad (1)$$

which leads to

$$D_N = \frac{ND_1}{1 + D_1(N-1)} \quad (2)$$

and

$$D_N = \frac{NM}{1 + NM} \quad D_1 = \frac{M}{1 + M} \quad (3)$$

Thus, D_N is larger than D_1 and permits a higher switching frequency to be used with transistors having given switching times.

Stress levels are also lower on some of the components, partly as a result of sharing between the extra elements when N is greater than unity. In particular, transistor Q_1 carries only the input current plus one N th of the output current, and the extra transistors carry only one N th of the output current. On the other hand, the voltage stress on Q_1 , which is $V_g/(1-D)$, is higher because of the higher D . The output diode still carries the sum of the input and output currents, but for a shorter fractional time $(1-D)$; its voltage stress level V/D is also lower.

Previously described extensions of the basic Ćuk converter can also be incorporated into the new circuit. For example, the input and output inductors may be coupled, with the attendant ripple steering properties [3]. Transformer isolation may be introduced between the two capacitors that result from splitting the first energy transfer capacitor into two in series [4], in which case all the magnetics may be integrated [5].

Of course, introduction of an isolation transformer may obviate the advantage obtained by the voltage divider circuitry, but it may be beneficial in some applications since the required transformer turns ratio would be smaller by the voltage division ratio. Also, in multiple outputs the relative volts per turn constraints would be eased. On the other hand, the dc isolation transformer would require separate drives for the first transistor on the primary side and for the others on the secondary side.

The small-signal model of the new voltage-divider Ćuk converter can be obtained by straightforward application of the state-space averaging analysis method [6]. The result is shown in Fig. 5 in two forms: in Fig. 5(a) the model is presented in the form that exposes the similarity to the

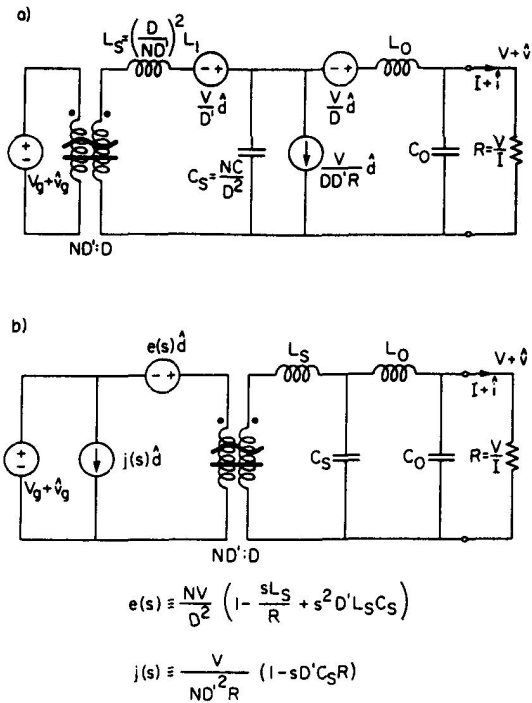


Fig. 5. Small-signal model of the N -stage voltage-divider Ćuk converter: (a) in form resembling that of a buck converter preceded by an input filter; (b) in canonical form.

model of the buck converter with input filter; in Fig. 5(b) the model is in the canonical form in which the modulation generators are in front of the two-section filter. As would be anticipated, both these forms are the same as for the original Ćuk converter except that certain element values are modified by the voltage-divider ratio N . Interpretation and utilization of both models have been extensively discussed elsewhere [7].

3. EXPERIMENTAL RESULTS

A three-stage voltage-divider Ćuk converter ($N = 3$) has been constructed to demonstrate feasibility. The circuit, shown in Fig. 6, is constructed on a printed circuit board with short length, large area connections. The circuit is designed for a nominal conversion ratio $M \equiv V/V_g = 5V/50V = 0.1$. Because only N -channel MOSFET transistors were conveniently available, the polarities are positive in, negative out. All the diodes are Schottkys.

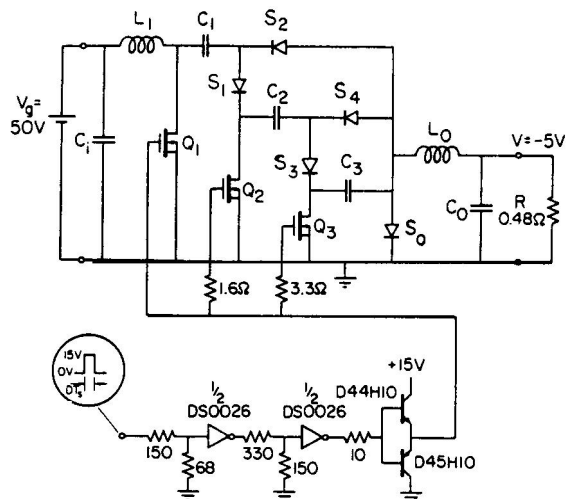


Fig. 6. Experimental 3-stage voltage-divider Ćuk converter operated at 500 kHz to 1 MHz.

The component list is as follows:

Q_1, Q_2, Q_3	RFP10N15 RCA N-channel MOSFET (150V, 10A, 0.3 Ω)
S_1, S_3, S_4	1N5822 (40V, 3A)
S_2	Fuji ERC88-009 (90V, 5A)
S_0	Unitrode USD945 (45V, 16A)
C_1, C_2, C_3	TRW-35 1 μ F 100V polypropylene, paralleled by 2 0.1 μ F ceramics
L_1	124 μ H 56 m Ω (25T #22 on Ferroxcube 1811 PA 250 387 pot core)
L_0	5 μ H 3 m Ω (6T 1.4 mm x 5.0 mm rectangular wire on Magnetics Inc. F material 1811 pot core)
C_0	100 μ F 35V, paralleled by a 1 μ F ceramic
C_i	1 μ F ceramic

The circuit operates as expected at a switching frequency of 500 kHz. The drain voltage V_{DS} and current I_D waveforms for each transistor are shown in Fig. 7. The calculated (ideal) duty ratio for $M = 0.1$ and $N = 3$ is

$$D_3 = \frac{NM}{1 + NM} = 0.23$$

compared with the value 0.28 observed in Fig. 7.

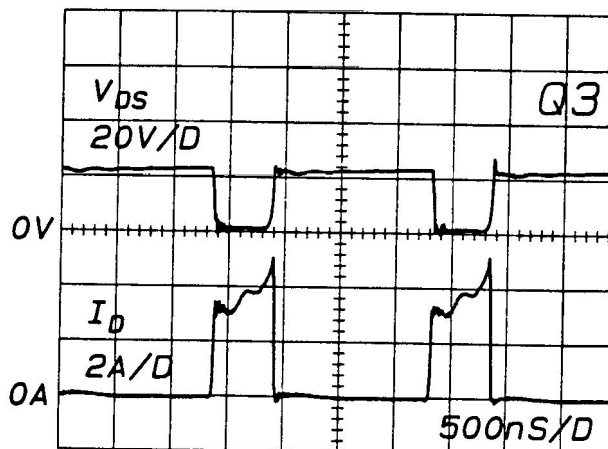
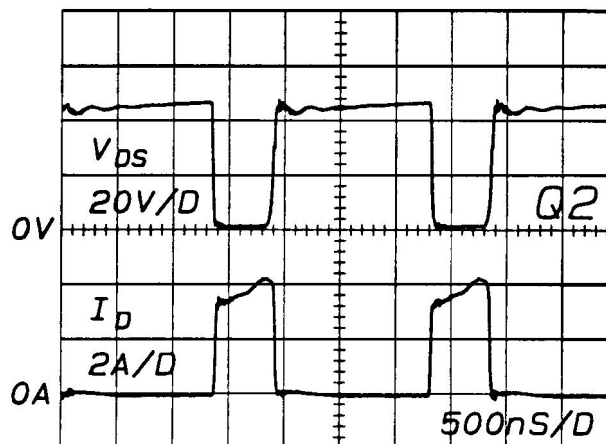
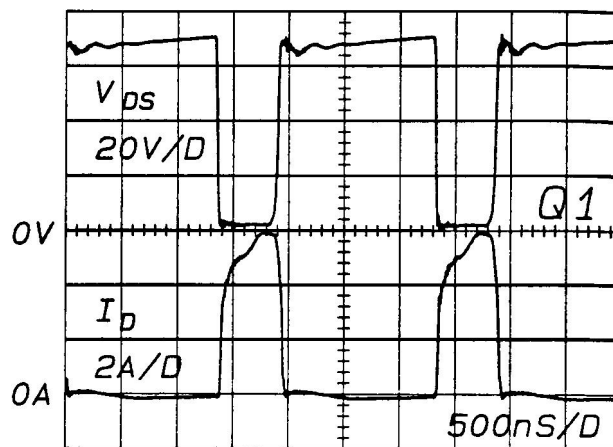


Fig. 7. Drain voltage V_{DS} and drain current I_D waveforms for the circuit of Fig. 6 operated at 500 kHz: (a) for Q_1 , (b) for Q_2 , (c) for Q_3 .

The waveforms shown in Fig. 7 are direct plots taken from a Tektronix 7854 digital sampling oscilloscope. The waveforms are quite clean, although ringing is very sensitive to the wire loop added for insertion of the current probe. All the voltage waveforms were taken without any such loops, and the current waveforms were taken with a loop only for the current being measured.

The overall efficiency at 500 kHz was measured to be 77%. For 5V out across a 0.48 Ω load, the output power is 52.1W and so the observed losses are 15.4W. A power loss budget was determined as follows:

	Loss	% of Total
Inductor resistances (apprx.)	0.5W	3%
Diode ON voltages	5.5W	35%
Transistor R_{Don} 's	3.9W	24%
Transistor switching	6.0W	38%
	15.9W	100%

The diode ON voltages were measured out of circuit, and R_{Don} was assumed to be 0.3 Ω . The transistor switching losses were calculated by the digital oscilloscope from the measured current and voltage waveforms (the 20ns delay in the current probe was accounted for).

The closeness of the budget losses of 15.9W to the observed overall loss of 15.4W provides reasonable assurance that the circuit operation is well understood. Further confirmation was obtained by operating the circuit under the same conditions, but at twice the switching frequency, 1 MHz. The observed efficiency was a little over 71%, corresponding to losses of 21.2W. On the assumption that the transistor switching losses double to 12.0W and the static losses remain the same, the budget losses increase to 21.9W, in good agreement with the observed value.

For comparison, a basic Ćuk converter without the voltage-divider feature was operated under the same conditions, namely, 50V in to 5V out at a 0.48 Ω load, at 500 kHz. The basic circuit was obtained by reconnection of the components on the N = 3 breadboard: the three transistors were connected in parallel, and the energy transfer capacitor consisted of C_1 and C_3 in parallel; C_2 and S_1 through S_4 were omitted.

The calculated duty ratio for M = 1 and N = 1 is

$$D_1 = \frac{M}{M+1} = 0.09$$

The measured drain voltage and current for the three paralleled transistors are shown in Fig. 8. The actual duty ratio is 0.11.

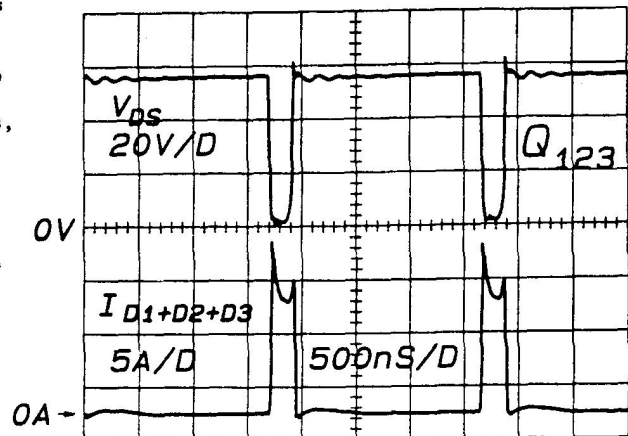


Fig. 8. Drain voltage and current waveforms for the three paralleled transistors when the circuit of Fig. 6 is reduced to a basic (single-stage) Ćuk converter.

The measured efficiency of the basic Ćuk converter at 500 kHz was 76%, marginally lower than the 77% of the three-stage divider Ćuk. However, at 1 MHz the efficiency of the basic Ćuk dropped to 67%, 4% less than the 71% of the three-stage circuit.

4. CONCLUSION

The voltage-divider Ćuk converter permits large overall step-down conversion ratios to be achieved without a transformer and yet with switch duty ratios that are not crunched at the low end, permitting higher switching frequencies to be used that take full advantage of power MOSFET fast switching speeds. Other advantages are that all the transistors have a common ground and can be driven in parallel from a single drive source, each additional transistor and shunt diode carries only one Nth of the output current, and each series diode carries only the input current. The circuit is particularly suitable for partial integration and hybrid construction techniques.

Experimental results confirm the basic operation, and show that the efficiency of a 50V to 5V 50W three-stage voltage-divider Ćuk converter was 77% at 500 kHz and 71% at 1 MHz, respectively 1% and 4% higher than the efficiency of a basic Ćuk converter operated at the same conditions.

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- [1] Vol. II, Sec. 18.
- [2] Vol. II, Sec. 27.
- [3] Vol. II, Secs. 19 and 20.
- [4] Vol. II, Secs. 22 and 26; Vol. III, Secs. 12 and 18.
- [5] Vol. II, Sec. 28; Vol. III, Secs. 2, 15, and 21.
- [6] Vol. I, Sec. 6.
- [7] Vol. II, Sec. 25.